1. (a) Design an expanding opcode with 12 bits in the instruction that will allow the following to be encoded. What is the maximum possible value of n? Explain why it is not good design practice to use this value. What is the maximum value of n consistent with good design of expanding opcodes?
- 6 instructions with three 3-bit registers
- 60 instructions with one 3-bit register
- n implicit /inherent instructions (no registers)

(b) A computer has 16 pages of virtual address space but only four page frames. Initially, the memory is empty. A program references the virtual pages in the order 0 7 2 7 5 8 9 2 4. Which references cause a page fault with LRU and which ones do so with FIFO?

2. (a) The Eight Queens Problem is a popular benchmark for evaluating the efficacy of speculative loading and branch predication (not branch prediction) in the IA-64 architecture. Go to the link on my homepage and find ONE solution in the format “46732815”. How many unique solutions exist? Who was the first mathematician to investigate this problem?

(b) At a certain point in time the diameter of a transistor was 1 micron. Invoke Moore’s Law to calculate the diameter of the same transistor two years earlier.

3. (a) What must be the range of decimal addresses if Port C of the 8255 PPI (#14) in the attached circuit is to be accessed?

(b) A 4-bit data word is Hamming coded. The received word is 1000110. What was the correct 4-bit data word actually sent?

4. Consider a “direct-mapped” cache consisting of 128 blocks of 16 bytes each for a total of 2KB. The main memory is 64KB, which can be viewed as 4K blocks of 16 bytes each. In this scheme block j of main memory maps onto block j modulo k of the cache.
(a) What is the value of k?
(b) In which block of the cache is block 257 from main memory stored?
(c) What replacement algorithm would be most efficient?
5. (a) Convert the following Java machine language program to IJVM Assembly. What is the outcome of the program segment?

\[
\begin{align*}
0x10 & 0x15 \\
0x10 & 0x60 \\
0x00 & 0x59 \\
0x60 & 0x00
\end{align*}
\]

(b) RAID level 3 is able to correct single-bit errors using only one parity drive. What is the point of RAID level 2? After all, it also can only correct one error and takes more drives to do so.

6. (a) The PCI 2.2 bus runs at 66 MHz and can handle 64-bit transfers. Calculate the percentage increase in bandwidth compared to the anachronistic ISA bus which runs at 8.33 MHz and can transfer 2 bytes per cycle.

(b) Convert the decimal number 26.725 to IEEE-754 32-bit format.

7. (a) An n-stage pipeline has the potential to increase the “throughput” (number of instructions executed per second) by a factor of n. However, factors such as cache misses and incorrect branch predictions can “stall” the pipeline. Consider a 4-stage pipeline in which the CPU clock is 100 MHz and the processor executes 100 MIPS (million instructions per second) when the pipeline does not install. Suppose the penalty for a stall is 17 clock cycles. Branch predictions are 95% accurate and cache misses occur 30% of the time. Calculate the throughput (in MIPS) for this CPU.

(b) What is the exact data capacity of a mode 2 CD-ROM containing the standard 74 minutes worth of data?

8. (a) The 3-variable multiplexer chip of Fig. 3-12 can be wired to implement a 4-variable Boolean function. Draw the logic diagram for the function that is 0 if the number has an even number of letters and 1 if the number has an odd number of letters (as spelled in English). For instance, 0111 is SEVEN which has 5 letters so the output function corresponding to 0111 is 1. Similarly the output corresponding to 1101 (THIRTEEN) is 0.

HINT: You will need a NOT gate in addition to the 74151 multiplexer.

L1. Write a 6800 code that will replace an even number with 0 and an odd number with 1.

L2. Write the Pentium Assembly Language code to replace a given even number with E and an odd number with D.