

In this lab you will be building and testing a full adder. You will be working in groups of three or four for this lab, one proto-board and two circuit boxes per group.

1. Using LogiSim, create a truth table for the full-adder. The inputs are  $C$ ,  $A$ , and  $B$ , in that order.  $C$  is the carry coming in,  $A$  and  $B$  are the input bits. The outputs are to be  $S$  and  $D$ , where  $S$  is the sum bit and  $D$  is the carry coming out of the adder.
2. Create the K-Map for each output.
3. Give the reduced SOP form of the output formulas.
4. Have LogiSim create the circuit, using just AND, OR, and NOT gates, with two inputs for the AND and OR gates.
5. Build the full adder on the proto-board. There are to be three inputs,  $S_1$ ,  $S_2$ , and  $S_3$ .  $S_1$  is the carry coming into the circuit ( $C$ ),  $S_2$  and  $S_3$  are the input bits ( $A$  and  $B$ ). There are two outputs, output 1 is the carry out ( $D$ ) and output 2 is the sum bit ( $S$ ).  
  
As usual, check the gates to make sure that they are functioning correctly. When you are finished, you will test the circuit for me. Be careful to remember which gates you took out of which box so that when you clean up, all of the boxes have the correct gates in them.
6. Using the Text Tool on LogiSim (**A**) on the tool bar, add the names of each member of your group to the circuit diagram. Save the circuit, File > Save, and then submit the file to the lab assignment. Hand in your written work, that is, the truth table, K-Maps, and SOP formulas, one copy per group.