1 Short Answer

Each question is worth 6 points.

1. Construct the truth tale for both the half adder and the full adder. Also, give their logical equations.

   Solution:

   Half-Adder

a	b	s	c
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

$$s = a'b + ab' \qquad c = ab$$

   Full-Adder

a	b	c_{in}	s	c_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	1	1	0
1	0	0	0	1
1	1	1	0	1
1	1	0	1	1

$$s = c'_{in}a'b + c'_{in}ab' + c_{in}a'b' + c_{in}ab \qquad c_{out} = c'_{in}ab + c_{in}a'b + c_{in}ab' + c_{in}ab = ab + c_{in}a + c_{in}b$$

2. Explain what an encoder circuit does. That is, what are the inputs, outputs, and function.

   Solution: There are 2^n inputs and n outputs. Which input channel is 1 generates a binary representation of that channel number for the output. So if channel 5 is a 1 then the output would be 101.

3. Explain what a decoder circuit does. That is, what are the inputs, outputs, and function.

   Solution: There are n inputs and 2^n outputs. The inputs are considered as a single binary number and the value of that number is the single output channel that will be 1, all other output channels will be 0. So of the input is 101, then output channel 5 will be a 1 and all others will be 0.

4. Explain what a multiplexer circuit does. That is, what are the inputs, outputs, and function.

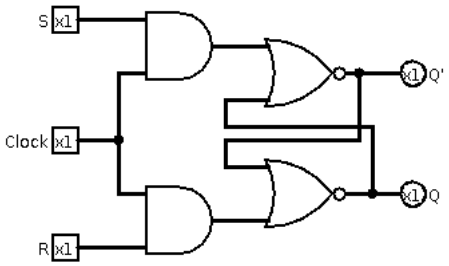
   Solution: There are 2^n input channels, one output channel, and n control signals. The control signals are considered as a single binary number and the value of that number is the input channel that will be sent to the output channel. So of the control signals are 101, then output will be the same as the input from channel 5.

5. Explain what a demultiplexer circuit does. That is, what are the inputs, outputs, and function.

   Solution: There are 2^n output channels, one input channel, and n control signals. The control signals are considered as a single binary number and the value of that number is the output channel that will be given the same value as the input channel. So if the control signals are 101, then output channel 5 will be the same as the input.

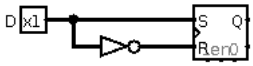
6. Draw the circuit diagram for a clocked SR flip-flop.

   Solution:



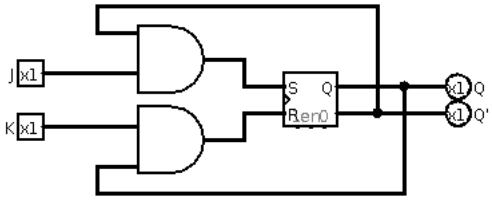
7. Using a clocked SR flip-flop, draw the diagram for a D flip-flop.

   Solution:



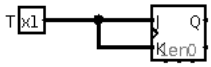
8. Using a clocked SR flip-flop, draw the diagram for a JK flip-flop.

   Solution:



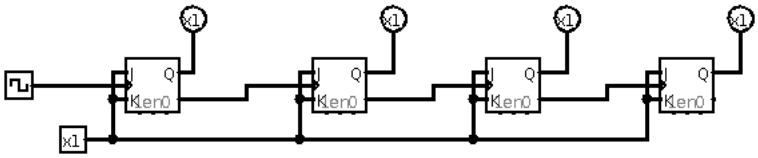
9. Using a clocked JK flip-flop, draw the diagram for a T flip-flop.

   Solution:



10. Using clocked JK flip-flops, construct a 4-bit counter.

    Solution:



2 Circuit Analysis

Do only one exercise in this section, it is worth 50 points.

11. For the following circuit, the top flip-flop is a T flip-flop and the bottom flip-flop is a JK flip-flop.

    (a) Create the transition tables for the two flip-flops.

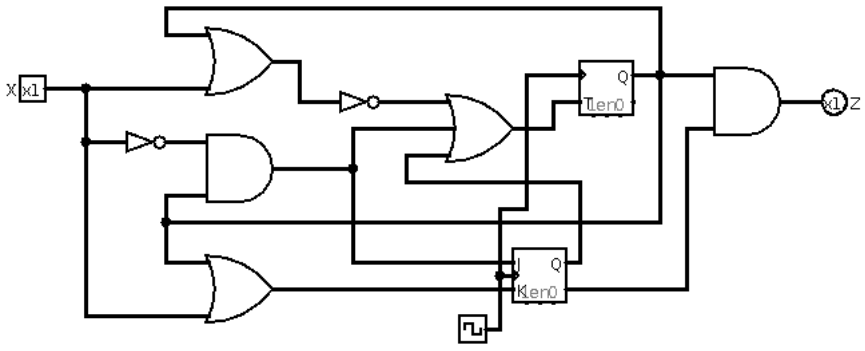
    (b) Create the transition table.

    (c) Create the next state table.

    (d) Create the output table.

    (e) Create the next state/output table.

    (f) Create the state diagram.



Solution:

T flip-flop (y_1): $T = (x + y_1)' + y_2 + x'y_1 = x' + y_2$

Input Table

	X	
y_1y_2	0	1
00	1	0
01	1	1
10	1	0
11	1	1

Transition Table

	X	
y_1y_2	0	1
00	1	0
01	1	1
10	0	1
11	0	0

JK flip-flop (y_2): $J = x'y_1 \qquad K = x + y_1$

Input Table for J

	X	
y_1y_2	0	1
00	0	0
01	0	0
10	1	0
11	1	0

Input Table for K

	X	
y_1y_2	0	1
00	0	1
01	0	1
10	1	1
11	1	1

Input Table for JK

	X	
y_1y_2	0	1
00	00	01
01	00	01
10	11	01
11	11	01

Transition Table

	X	
y_1y_2	0	1
00	0	0
01	1	0
10	1	0
11	0	0

Circuit Tables

State Transition Table

	X	
y_1y_2	0	1
00	10	00
01	11	10
10	01	10
11	00	00

Next State Table

	X	
	0	1
A	C	A
B	D	C
C	B	C
D	A	A

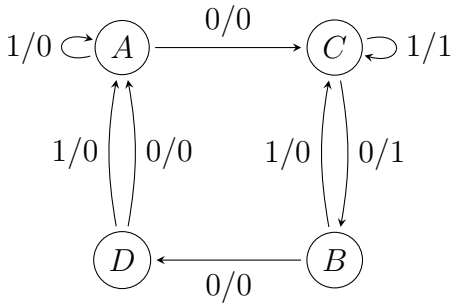
Output Table

	X	
y_1y_2	0	1
00	0	0
01	0	0
10	1	1
11	0	0

Next State/Output Table

	X	
	0	1
A	C/0	A/0
B	D/0	C/0
C	B/1	C/1
D	A/0	A/0

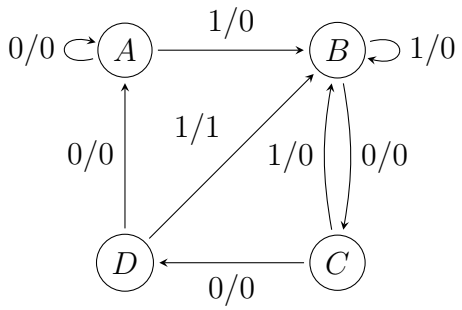
State Diagram



12. Design a sequential circuit that detects an input sequence of 1001 with overlap. Use only JK flip-flops in your construction.

Solution:

State Diagram



Circuit Tables

Next State/Output Table

	X = 0	X = 1
A	A/0	B/0
B	C/0	B/0
C	D/0	B/0
D	A/0	B/1

Next State Table

	X = 0	X = 1
A	A	B
B	C	B
C	D	B
D	A	B

State Transition Table

y_1y_2	X = 0	X = 1
00	00	01
01	10	01
10	11	01
11	00	01

Output Table $Z = xy_1y_2$

y_1y_2	X = 0	X = 1
00	0	0
01	0	0
10	0	0
11	0	1

JK flip-flop (y_1): $J_1 = x'y_2$ $\quad K_1 = y_1x + y_1y_2$

Transition Table

y_1y_2	X = 0	X = 1
00	0	0
01	1	0
10	1	0
11	0	0

Input Table for JK

y_1y_2	X = 0	X = 1
00	0d	0d
01	1d	0d
10	d0	d1
11	d1	d1

Input Table for J

y_1y_2	X = 0	X = 1
00	0	0
01	1	0
10	d	d
11	d	d

Input Table for K

y_1y_2	X = 0	X = 1
00	d	d
01	d	d
10	0	1
11	1	1

JK flip-flop (y_2): $J_2 = x + y_1y_2'$ $\quad K_2 = x'$

Transition Table

y_1y_2	X = 0	X = 1
00	0	1
01	0	1
10	1	1
11	0	1

Input Table for JK

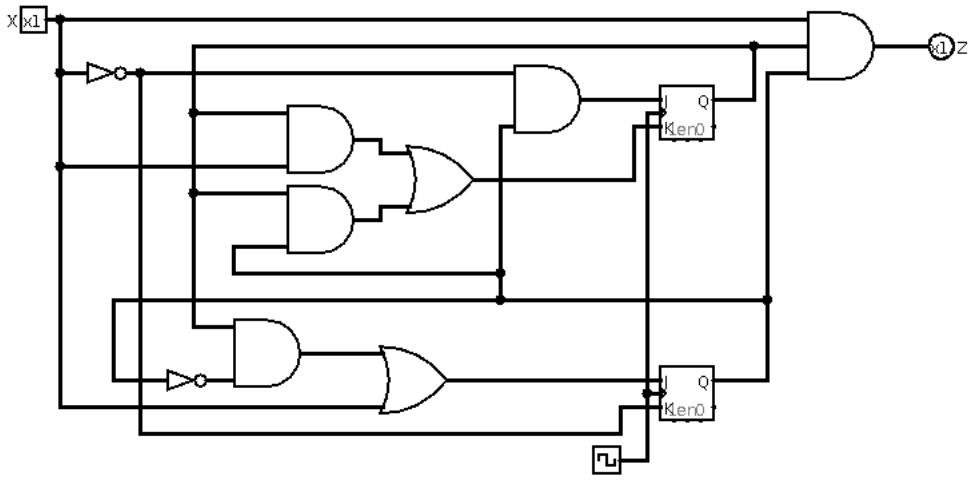
y_1y_2	X = 0	X = 1
00	0d	1d
01	d1	d0
10	1d	1d
11	d1	d0

Input Table for J

y_1y_2	X = 0	X = 1
00	0	1
01	d	d
10	1	1
11	d	d

Input Table for K

y_1y_2	X = 0	X = 1
00	d	d
01	1	0
10	d	d
11	1	0



Flip-Flop Characteristic Tables

$Q(t)$	SR	$Q(t+1)$
0	00	0
0	01	0
0	10	1
0	11	—
1	00	1
1	01	0
1	10	1
1	11	—

$Q(t)$	JK	$Q(t+1)$
0	00	0
0	01	0
0	10	1
0	11	1
1	00	1
1	01	0
1	10	1
1	11	0

$Q(t)$	D	$Q(t+1)$
0	0	0
0	1	1
1	0	0
1	1	1

$Q(t)$	T	$Q(t+1)$
0	0	0
0	1	1
1	0	1
1	1	0

Flip-Flop Excitation Tables

$Q(t)$	$Q(t+1)$	SR	D	JK	T
0	0	0d	0	0d	0
0	1	10	1	1d	1
1	0	01	0	d1	1
1	1	d0	1	d0	0