1 Short Answer

Each question is worth 10 points.

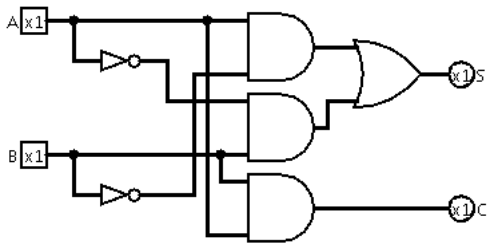
1. Construct the truth table, logical expressions, and circuit (using AND, OR , and NOT gates) for the half-adder.

   Solution:

   Half-Adder

a	b	s	c
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

$s = a'b + ab'$ $\qquad$ $c = ab$



2. Construct the truth table and logical expressions for the full-adder.

   Solution:

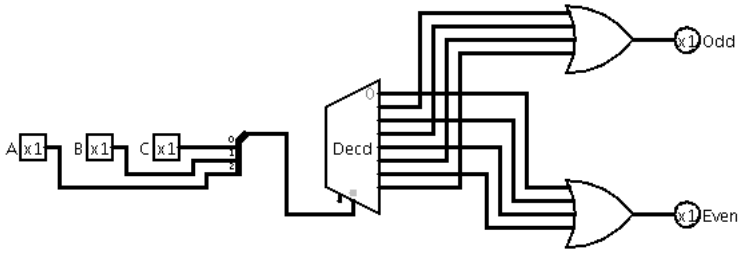
   Full-Adder

a	b	c_{in}	s	c_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$s = c'_{in}a'b + c'_{in}ab' + c_{in}a'b' + c_{in}ab$ $\qquad$ $c_{out} = c'_{in}ab + c_{in}a'b + c_{in}ab' + c_{in}ab = ab + c_{in}a + c_{in}b$

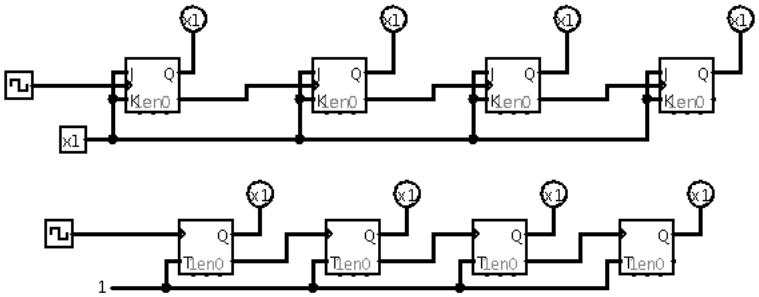
3. Use a 3-8 decoder to create a circuit with three inputs A, B, and C (thought of as the binary number ABC) and two outputs, Even and Odd. If the number ABC is even the Even output should be 1 and the Odd output should be 0. Similarly, if the number ABC is odd the Even output should be 0 and the Odd output should be 1.

   Solution:



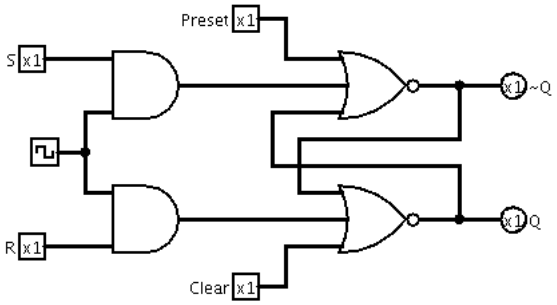
4. Construct two clocked 4-bit counters, one using JK flip-flops and the other using T flip-flops.

   Solution:



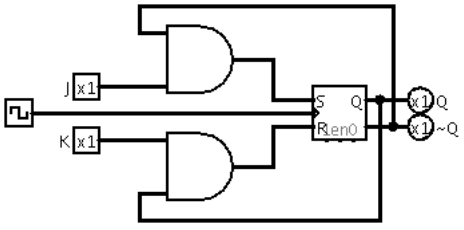
5. Draw the circuit diagram for a clocked SR flip-flop, with asynchronous preset and clear. Use only NOR and AND gates.

   Solution:



6. Using and SR flip-flop and AND gates create a clocked JK flip-flop.

   Solution:



2 Circuit Analysis

Do only one exercise in this section, it is worth 50 points.

7. For the following circuit, the top flip-flop is a JK flip-flop and the bottom flip-flop is a T flip-flop.

   (a) Create the transition tables for the two flip-flops.

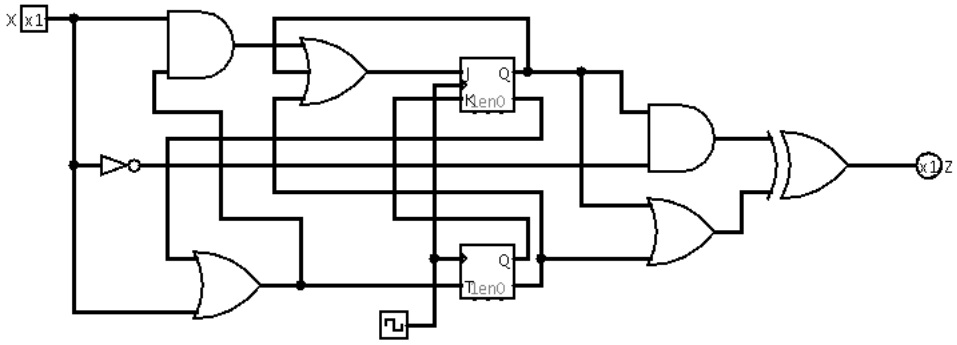
   (b) Create the transition table.

   (c) Create the next state table.

   (d) Create the output table.

   (e) Create the next state/output table.

   (f) Create the state diagram.



Solution:

JK flip-flop (Q_1):

$J = x(x + Q_1') + Q_1 + Q_2' = x + xQ_1' + Q_1 + Q_2'$

$K = Q_2$

Input Table for J

	X	
Q_1Q_2	0	1
00	1	1
01	0	1
10	1	1
11	1	1

Input Table for K

	X	
Q_1Q_2	0	1
00	0	0
01	1	1
10	0	0
11	1	1

Input Table for JK

	X	
Q_1Q_2	0	1
00	10	10
01	01	11
10	10	10
11	11	11

Transition Table

	X	
Q_1Q_2	0	1
00	1	1
01	0	1
10	1	1
11	0	0

T flip-flop (Q_2): $T = x + Q_1'$

Input Table

	X	
Q_1Q_2	0	1
00	1	1
01	1	1
10	0	1
11	0	1

Transition Table

	X	
Q_1Q_2	0	1
00	1	1
01	0	0
10	0	1
11	1	0

Circuit Tables

State Transition Table

	X	
Q_1Q_2	0	1
00	11	11
01	00	10
10	10	11
11	01	00

Next State Table

	X	
	0	1
A	D	D
B	A	C
C	C	D
D	B	A

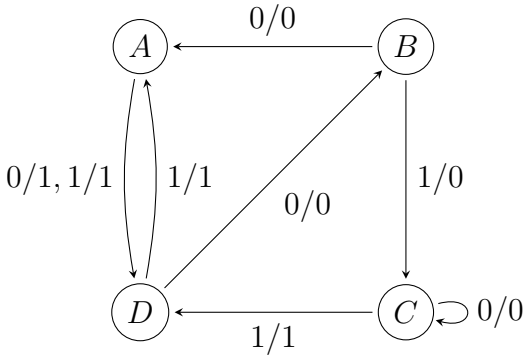
Output Table

	X	
Q_1Q_2	0	1
00	1	1
01	0	0
10	0	1
11	0	1

Next State/Output Table

	X	
	0	1
A	D/1	D/1
B	A/0	C/0
C	C/0	D/1
D	B/0	A/1

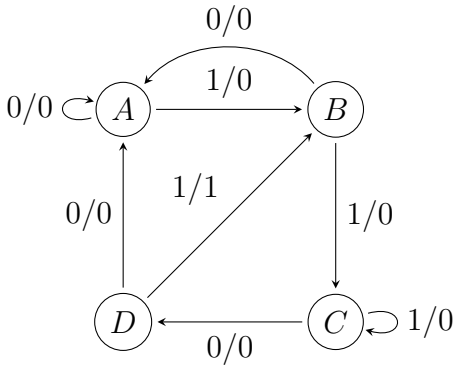
State Diagram



8. Design a sequential circuit that detects an input sequence of 1101 with overlap. Use only JK flip-flops in your construction.

Solution:

State Diagram



Circuit Tables

Next State/Output Table

	X = 0	X = 1
A	A/0	B/0
B	A/0	C/0
C	D/0	C/0
D	A/0	B/1

Next State Table

	X = 0	X = 1
A	A	B
B	A	C
C	D	C
D	A	B

State Transition Table

Q_1Q_2	X = 0	X = 1
00	00	01
01	00	10
10	11	10
11	00	01

Output Table $Z = xQ_1Q_2$

Q_1Q_2	X = 0	X = 1
00	0	0
01	0	0
10	0	0
11	0	1

JK flip-flop (Q_1): $J_1 = xQ_2$ $K_1 = Q_2$

Transition Table

Q_1Q_2	X = 0	X = 1
00	0	0
01	0	1
10	1	1
11	0	0

Input Table for JK

Q_1Q_2	X = 0	X = 1
00	0d	0d
01	0d	1d
10	d0	d0
11	d1	d1

Input Table for J

Q_1Q_2	X = 0	X = 1
00	0	0
01	0	1
10	d	d
11	d	d

Input Table for K

Q_1Q_2	X = 0	X = 1
00	d	d
01	d	d
10	0	0
11	1	1

JK flip-flop (Q_2): $J_2 = x'Q_1 + xQ_1'$ $K_2 = x' + Q_1'$

Transition Table

Q_1Q_2	X = 0	X = 1
00	0	1
01	0	0
10	1	0
11	0	1

Input Table for JK

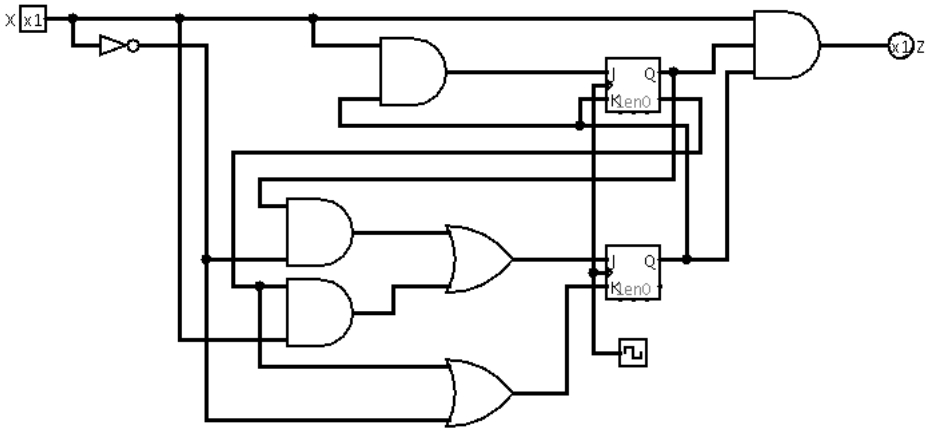
Q_1Q_2	X = 0	X = 1
00	0d	1d
01	d1	d1
10	1d	0d
11	d1	d0

Input Table for J

Q_1Q_2	X = 0	X = 1
00	0	1
01	d	d
10	1	0
11	d	d

Input Table for K

Q_1Q_2	X = 0	X = 1
00	d	d
01	1	1
10	d	d
11	1	0



Flip-Flop Characteristic Tables

$Q(t)$	SR	$Q(t+1)$
0	00	0
0	01	0
0	10	1
0	11	—
1	00	1
1	01	0
1	10	1
1	11	—

$Q(t)$	JK	$Q(t+1)$
0	00	0
0	01	0
0	10	1
0	11	1
1	00	1
1	01	0
1	10	1
1	11	0

$Q(t)$	D	$Q(t+1)$
0	0	0
0	1	1
1	0	0
1	1	1

$Q(t)$	T	$Q(t+1)$
0	0	0
0	1	1
1	0	1
1	1	0

Flip-Flop Excitation Tables

$Q(t)$	$Q(t+1)$	SR	D	JK	T
0	0	0d	0	0d	0
0	1	10	1	1d	1
1	0	01	0	d1	1
1	1	d0	1	d0	0