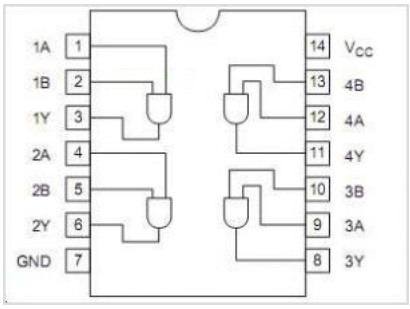
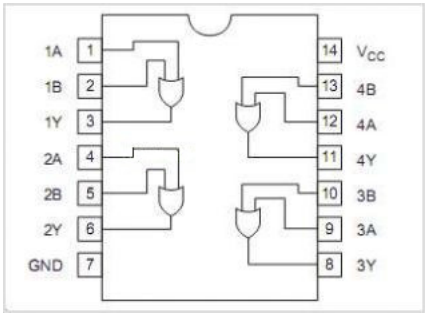
Chip Logic

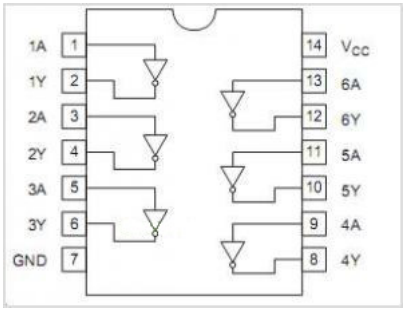
AND Gates — HD74LS08P These devices contain four independent 2-input AND Gates, they perform the Boolean functions in positive Logic; $Y = AB$.



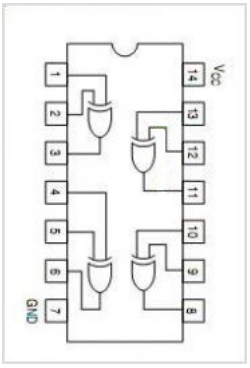
OR Gates — HD74LS32P These devices contain four independent 2-input OR Gates, they perform the Boolean functions in positive Logic; $Y = A + B$.



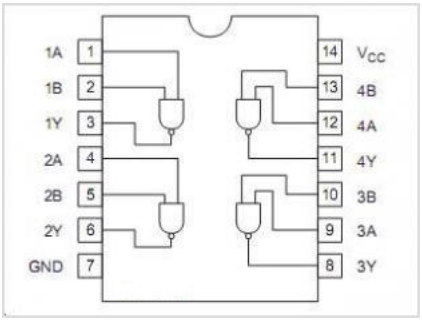
NOT Gates — HD74LS04P These devices contain four independent 1-input NOT Gates, they perform the Boolean functions in positive Logic; $Y = \overline{A}$.



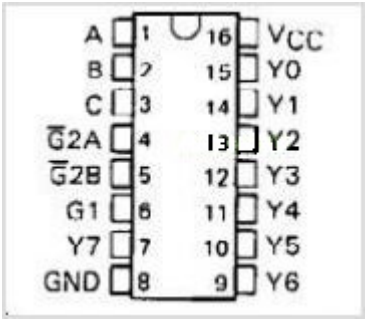
XOR Gates — SN74LS86AN These devices contain four independent 2-input Exclusive-OR Gates, they perform the Boolean functions in positive Logic, $Y = A \oplus B = \overline{A}B + A\overline{B}$



NAND Gates — HD74LS00P These devices contain four independent 2-input NAND Gates, they perform the Boolean functions in positive Logic, $Y = \overline{AB} = \overline{A} + \overline{B}$



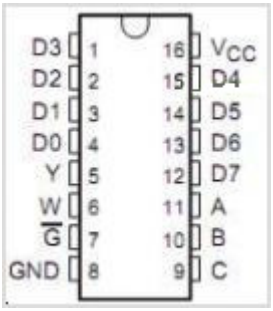
3-Line to 8-Line Decoder / Demultiplexer — SN74LS138N The SN74S138N will decode one of eight lines dependent on the conditions at the three binary select inputs and the three enable inputs.



Function Table: H = High, L = Low, X = Irrelevant, $G2 = \overline{G2A} + \overline{G2B}$

Inputs					Outputs							
Enable		Select										
G1	G2	A	B	C	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	H	L	L	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

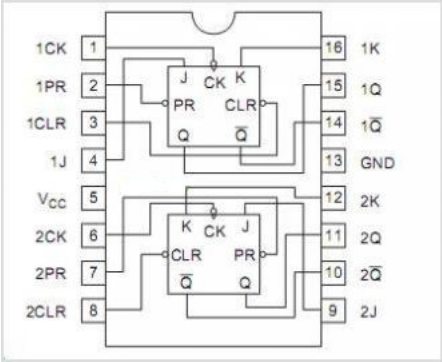
8-Line To 1-Line Data Selectors/Multiplexers — SN74LS151N The SN74LS151N will select one of eight lines dependent on the conditions at the three binary select inputs.



Function Table: H = High, L = Low, X = Irrelevant, $W = \overline{Y}$.

Inputs				Outputs	
Select			Strobe		
A	B	C	$\overline{G}$	Y	W
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
H	L	L	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
H	H	L	L	D3	$\overline{D3}$
L	L	H	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
L	H	H	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

Dual J-K Flip-Flops with Preset And Clear — SN74LS74AN Dual J-K Flip-Flops.



Dual D-type Pos-Edge-Triggered Flip-Flops with Preset And Clear — SN74LS74AN

These devices contain two independent D-type positive-edge-triggered Flip-Flops A low level at the preset or clear inputs sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the D input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the Clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the Clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.